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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/828,983	RAPAICH, MARK	
	Examiner	Art Unit	
	Joseph Schell	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-11 and 13-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-11 and 13-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claims 1, 4-11 and 13-31 have been examined.

Claims 1, 4-11 and 13-31 have been rejected.

Response to Arguments

1. The arguments submitted August 20, 2007 have been fully considered but are unpersuasive.

2. Applicant argues that Lin ('695) does not teach turning off a visual indicator when no faults are detected. Applicant argues that because the indicator serves as the power LED to indicate power, it is not turned off when no faults are detected. The examiner respectfully disagrees. To "turn off" and "turn on" a visual indicator are general terms. When the indicator sequentially indicates multiple errors, as in the case of the LED in Lin ('695), to "turn on the visual indicator" can mean the indicator receives power, or the indicator activates to indicate one or multiple errors. To "turn off the visual indicator" can mean the removal of power, or the ceasing of indicating one or multiple errors. To "turn off" can refer to any aspect of the visual indicator. As shown in Figures 5a and 5b, Lin ('685) successively performs tests and uses the LED to indicate errors. The LED thus indicates "error" or "no error" for each test, and when done with a particular test (at steps 506, 508 and 512) the particular testing aspect of the LED is deactivated in favor of indicating results for the next test.

3. Applicant argues that because a viewer in Lin ('695) can not distinguish error-free test results from no more tests, Lin ('695) does not teach turning off a visual indicator when no faults are detected, as claimed. The examiner respectfully disagrees. As shown in Figures 5a and 5b, the LED blinks at different frequencies depending on the error type (elements 505, 508 and 511). When the LED blinks at the second frequency, the aspect of the LED indicating RAM test failures has been deactivated.

4. Applicant argues that Lin ('695) does not teach diagnostic testing of a computer motherboard prior to detecting faults in a memory subsystem. This argument is moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 4-7, 9-11, 13-15, 17, 19-21, 23-25, and 29-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin (US Patent 6,862,695).

6. As per claim 1, Lin ('695) discloses an apparatus for detecting and indicating faults on a computer motherboard comprising:

a nonvolatile memory device for storing a plurality of diagnostic instructions for detecting faults on said computer motherboard (column 2 lines 30-36, test instructions are stored in the BIOS); and

a microprocessor, coupled to said nonvolatile memory device, for, responsive to receiving an initialization signal (as shown in Figure 5a, the computer power on begins the POST), requesting and retrieving said plurality of diagnostic instructions, and executing the diagnostic instructions so as to detect faults on said computer motherboard (column 2 lines 26-35, it's referred to as "a device" but it executes BIOS instructions, thus it is a processor); and

a visual indicator coupled to and controlled by said microprocessor for providing a visual indication when a fault on said computer motherboard is detected during execution of said diagnostic instructions by the microprocessor (as shown in Figure 5a steps 504 and 505);

wherein said microprocessor is configured by said plurality of diagnostic instructions to:

first turn on a visual indicator when power is applied to said computer motherboard (column 3 line 65 through column 4 line 1, among other things the LED acts as an indicator of system power status. This aspect is turned on when power is applied);

execute a first portion of said plurality of diagnostic instructions so as to detect faults on said computer motherboard (Figure 5a element 504);

second turn off said visual indicator when no faults on said computer motherboard are detected during execution of said diagnostic instructions (as shown in Figure 5a and 5b, when no failures are encountered during RAM tests, the system tests BIOS. At that time the LED stops acting as a visual indicator of RAM failure and begins acting as a visual indicator of BIOS error).

As per claim 4, Lin ('695) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1, further comprising a flash circuit for flashing said visual indicator upon detection of a fault on a memory subsystem (column 3 lines 5-10).

7. As per claim 5, Lin ('695) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1, wherein said nonvolatile memory device stores power-on self-test diagnostic instructions and basic input and output system instructions (column 4 lines 7-10 and 12-14, BIOS are utilized during the POST, and column 4 lines 38-45, the BIOS are verified by the POST).

8. As per claim 6, Lin ('695) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1 wherein said visual indicator is a light emitting diode (column 4 lines 61-64).

9. As per claim 7, Lin ('695) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1 wherein said visual indicator is an

external visual indicator (as shown in Figure 3, the LED is externally connected through an I/O port).

10. As per claim 9, Lin ('695) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 7, further comprising an I/O port coupled to said microprocessor, said microprocessor providing signals to said external visual indicator via said I/O port (as shown in Figure 3, the LED receives signals via an I/O port).

11. As per claim 10, Lin ('695) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1, wherein said computer motherboard includes integrated circuits mounted on said computer motherboard (as shown in Figures 6a and 6b, the POST tests RAM, BIOS and display adapter).

12. As per claim 11, Lin ('695) discloses a method for detecting and indicating that there are no faults on a computer motherboard comprising the steps of:

storing in a nonvolatile memory device a plurality of diagnostic instructions for detecting faults on said computer motherboard (column 2 lines 30-36, test instructions are stored in the BIOS);

receiving an initialization signal to start a computer system (as shown in Figure 5a, the computer power on begins the POST);

turning on a visual indicator when power is applied to said computer motherboard (column 3 line 65 through column 4 line 1, among other things the LED acts as an indicator of system power status. This aspect is turned on when power is applied);

requesting and retrieving said diagnostic instructions, and first executing a first portion of said diagnostic instructions so as to detect faults on said computer motherboard, responsive to reception of said initialization signal (Figure 5a, element 504);

turning off said visual indicator when no faults on said computer motherboard are detected during execution of said diagnostic instructions (as shown in Figure 5a and 5b, when no failures are encountered during RAM tests, the system tests BIOS. At that time the LED stops acting as a visual indicator of RAM failure and begins acting as a visual indicator of BIOS error);

initializing a memory subsystem (Figure 5b, element 506);

second executing a second portion of said diagnostic instructions so as to detect faults in said memory subsystem (Figure 5b, element 507); and

flashing said visual indicator when a fault is found on said memory subsystem (Figure 5a element 508).

13. As per claims 13-15 and 17, these claims recite limitations found in claims 5-7 and 9, respectively, and are respectively rejected on the same grounds as claims 4-7 and 9.

14. As per claim 19, 21, 23, 24, and 25, this claims recites limitations found in claims 11, 15, 13, 14 and 17, respectively, and are respectively rejected on the same grounds as claims 11, 15, 13, 14 and 17.

15. As per claim 20, this claim recites limitations found in claim 11 and is rejected on the same grounds as claim 11.

16. As per claim 29, Lin ('695) discloses the method for detecting and indicating faults on a computer motherboard as in claim 11, wherein said visual indicator remains turned on when faults are detected on said computer motherboard (column 2 line 53 "eventually" the third hardware device is tested, the blinking from an error indication continues until this eventuality is reached).

17. As per claim 30, Lin ('695) discloses the method for detecting and indicating faults on a computer motherboard as in claim 11, wherein

said visual indicator remains turned on at least until said first portion of said diagnostic instructions are executed (column 3 line 65 through column 4 line 2, the LED acts as a power indicator, and column 4 lines 32-37 during the POST of RAM, the LED is active to indicate any detected errors in the RAM), and

remains turned on if faults are detected on said computer motherboard (column 2 line 53 "eventually" the third hardware device is tested, the blinking from an error indication continues until this eventuality is reached).

18. As per claim 31, Lin ('695) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1, wherein said microprocessor is further configured by said plurality of diagnostic instructions to:

initialize a memory subsystem (Figure 5a, POST is an initializing process because it is done before the RAM is put to use);

execute a second portion of said diagnostic instructions so as to detect faults in said memory subsystem (Figure 5a, element 504); and

flash said visual indicator when a fault is found on said memory subsystem (Figure 5a element 505).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 8, 16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin ('695) in view of BOXX Box Boxes Clever.

20. As per claim 8, Lin ('695) discloses the apparatus for detecting and indicating faults in a computer motherboard as in claim 1. Lin ('695) does not explicitly disclose the apparatus wherein said visual indicator is an internal visual indicator.

BOXX Box Boxes Clever is a review of a computer casing.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Lin ('695) such that when they are unneeded, the diagnostic LEDs can be concealed. This modification would have been obvious because bright LEDs can be so annoying to a casual computer user that he may attempt to manually conceal them (BOXX Box Boxes Clever, third paragraph from the end).

21. As per claims 16 and 22, these claims recite limitations found in claim 8 and are rejected on the same grounds as claim 8.

22. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin ('695) in view of BIOS Beep Codes.

Lin ('695) discloses the method for detecting and indicating faults on a computer motherboard as in claim 11, wherein said computer motherboard includes integrated circuits mounted on said computer motherboard (as shown in Figures 6a and 6b, BIOS and display adapter).

Lin ('695) does not expressly disclose the system wherein the POST sequence tests multiple motherboard subsystems beyond the RAM of Lin ('695).

BIOS Beep Codes decodes the meaning of beep failures occurring during a PC POST.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Lin ('695) such that multiple motherboard subsystems are checked for error. This modification would have been obvious because AMI BIOS is one of the most popular in the PC world (BIOS Beep Codes, main frame of main page) and it includes tests for DRAM (1 beep), parity circuitry (2 beeps), base RAM (3 beeps), ROM BIOS (9 beeps), cache memory (11 beeps), and various hardware (4, 5, 8, 10 beeps) (all beep count identifiers as shown in BIOS Beep Codes, side frame).

23. Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin ('695) in view of BIOS Power-On Self Test.

24. As per claim 26, Lin ('695) discloses an apparatus for detecting and indicating faults on a computer motherboard and in a memory subsystem of a computer system comprising:

an external visual indicator (see Figure 3);

a general I/O port coupled to said visual indicator (see Figure 3);

a flash circuit coupled to said visual indicator for flashing said visual indicator (column 4 lines 35-37, a control signal is used to control the LED flashing, this inherently requires circuitry);

a host bus for transmitting address and data signals (see Figure 3);

a nonvolatile memory device coupled to said host bus storing a plurality of diagnostic instructions, said plurality of diagnostic instructions including power-on self-test diagnostic instructions for detecting faults in said computer motherboard and in a memory subsystem (the BIOS of figure 3, also see column 4 lines 7-10 and 12-14, BIOS are utilized during the POST, and column 4 lines 38-45, the BIOS are verified by the POST);

a microprocessor coupled to said bus, to said I/O port, and to said flash circuit, said microprocessor turning said visual indicator on through said general I/O port and requesting and retrieving said plurality of diagnostic instructions upon reception of an initialization signal to start said computer system, executing said diagnostic instructions for detecting faults in said computer motherboard and executing said diagnostic instructions for detecting faults in said memory subsystem, turning said visual indicator off if no faults are detected in said computer motherboard, and activating said flash circuit if faults are detected in said memory subsystem (column 2 line 62 through column 3 line 11, and see Figure 5a wherein the computer power on triggers the POST and the POST tests RAM and in Figure 5b where the POST tests BIOS).

Lin ('695) teaches detecting faulty RAM followed by detecting faults in BIOS, followed by other POST routines (Figures 5a and 5b).

Lin ('695) does not expressly disclose the system comprising executing diagnostic instructions for detecting faults in a computer motherboard prior to executing diagnostic instructions for detecting faults in a memory subsystem.

BIOS Power-On Self Test teaches a BIOS POST sequence wherein the POST first checks that hardware is present and functioning properly and later tests memory (first paragraph).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the diagnostic system disclosed by Lin ('695) such that an initial part of the POST sequence checks the system hardware, as taught by BIOS Power-On Self Test, before testing RAM as taught in Lin ('695). This modification would have been obvious because it is the typical PC booting sequence (BIOS Power-On Self Test first paragraph).

25. As per claim 27, Lin ('695) BIOS Power-On Self Test discloses the apparatus for detecting and indicating faults on a computer motherboard and in a memory subsystem of a computer system as in claim 26, wherein said external visual indicator is located on a panel of said computer system (column 3 line 65 through column 4 line 1).

26. As per claim 28, Lin ('695) BIOS Power-On Self Test discloses the apparatus for detecting and indicating faults on a computer motherboard and in a memory subsystem of a computer system as in claim 26, wherein said computer motherboard comprises an integrated circuit mounted on said computer motherboard (as shown in Figures 5a and 5b, the POST tests RAM, BIOS and a Display Adapter).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Schell whose telephone number is (571) 272-8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS

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